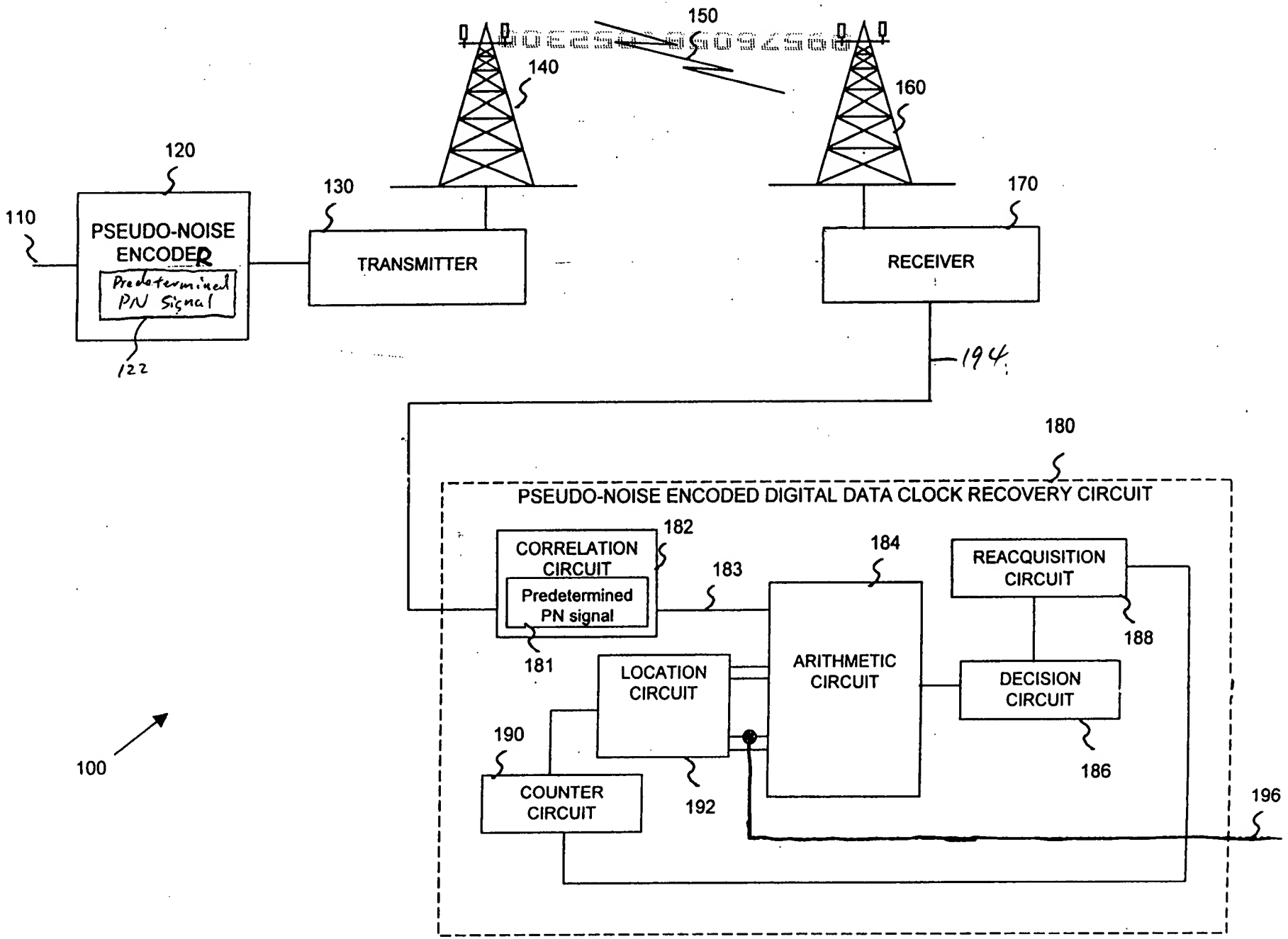

150
140
160
120
130
170
110
PSEUDO-NOISE ENCODER
Predetermined PN Signal
TRANSMITTER
RECEIVER
122
194
180
PSEUDO-NOISE ENCODED DIGITAL DATA CLOCK RECOVERY CIRCUIT
CORRELATION CIRCUIT
Predetermined PN signal
182
183
184
REACQUISITION CIRCUIT
188
181
LOCATION CIRCUIT
ARITHMETIC CIRCUIT
DECISION CIRCUIT
186
190
COUNTER CIRCUIT
192
196
100

Fig. 1

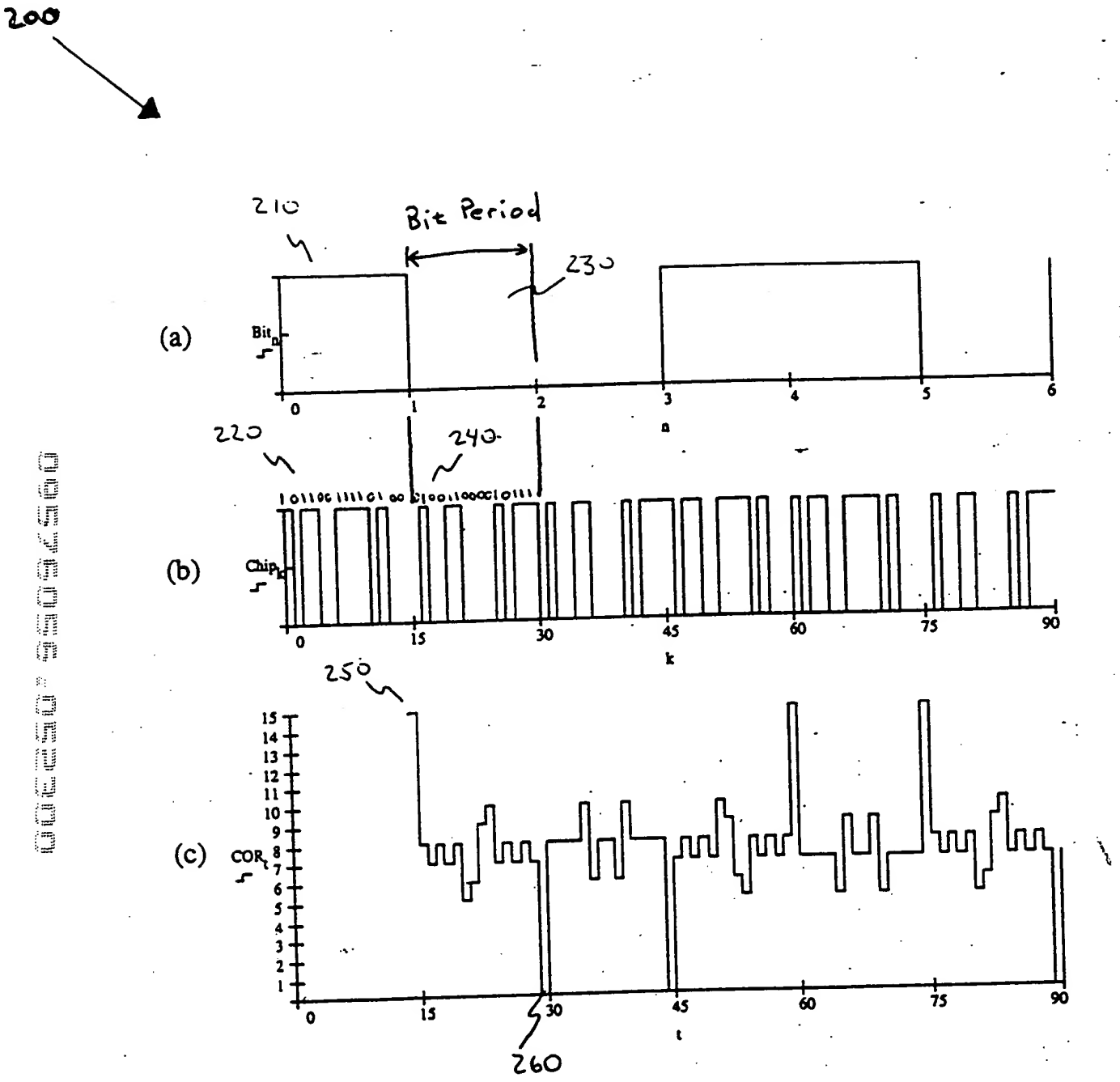

200
210
Bit Period
230
(a)
Bit_n
0
1
2
3
4
5
6
n
220
240
(b)
Chip_k
0
15
30
45
60
75
90
k
250
(c)
COR_t
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
15
30
45
60
75
90
t
260

Fig. 2

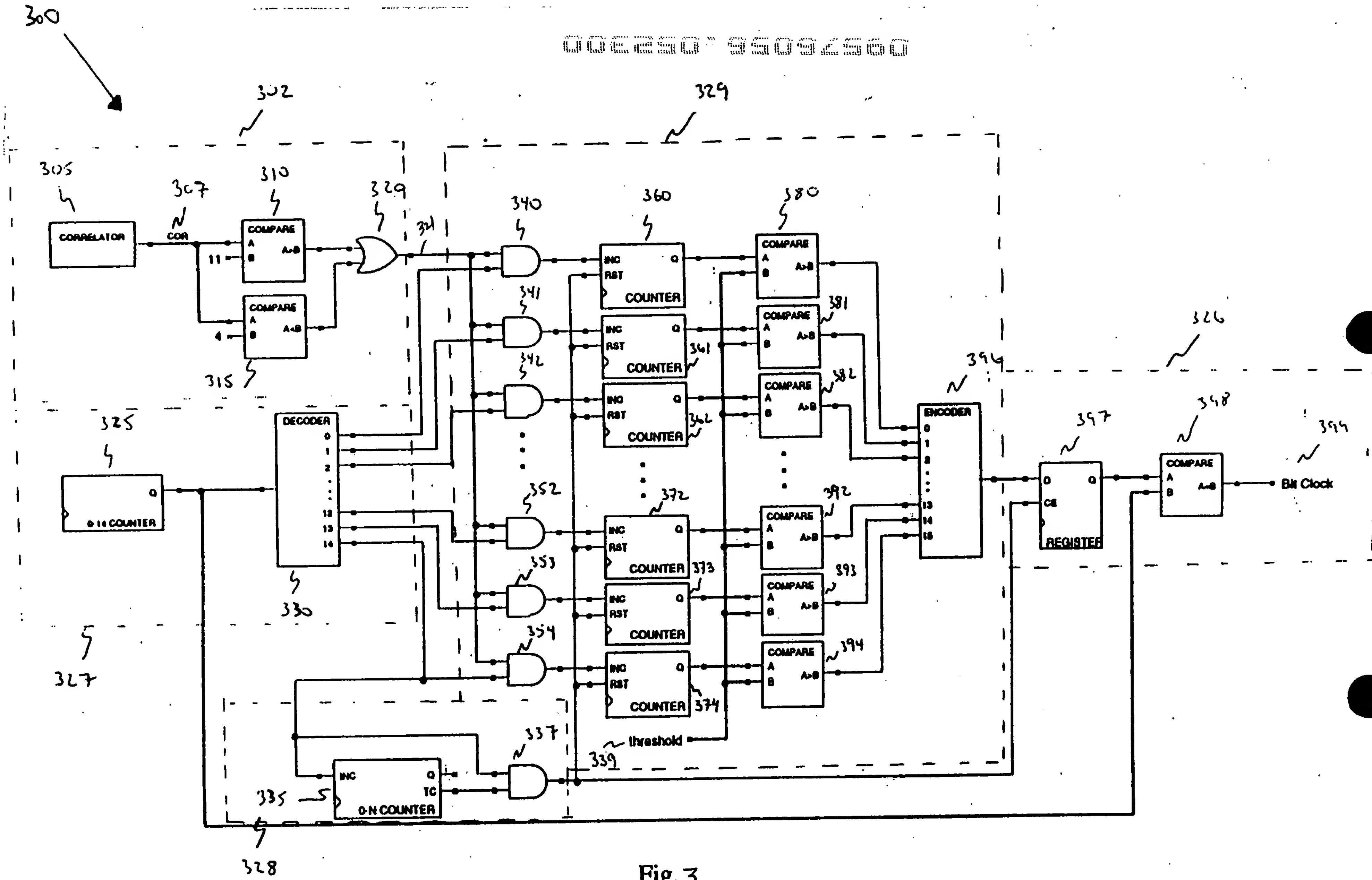

300
302
329
305
307
310
329
341
340
360
380
CORRELATOR
COR
COMPARE
A
B
A>B
11
4
A<B
315
341
361
381
COUNTER
INC
RST
Q
342
362
382
325
0-14 COUNTER
DECODER
0
1
2
12
13
14
330
352
372
392
353
373
393
354
374
394
326
396
397
398
399
ENCODER
15
REGISTER
D
Q
CE
Bit Clock
threshold
339
337
335
0-N COUNTER
TC
327
328

Fig. 3

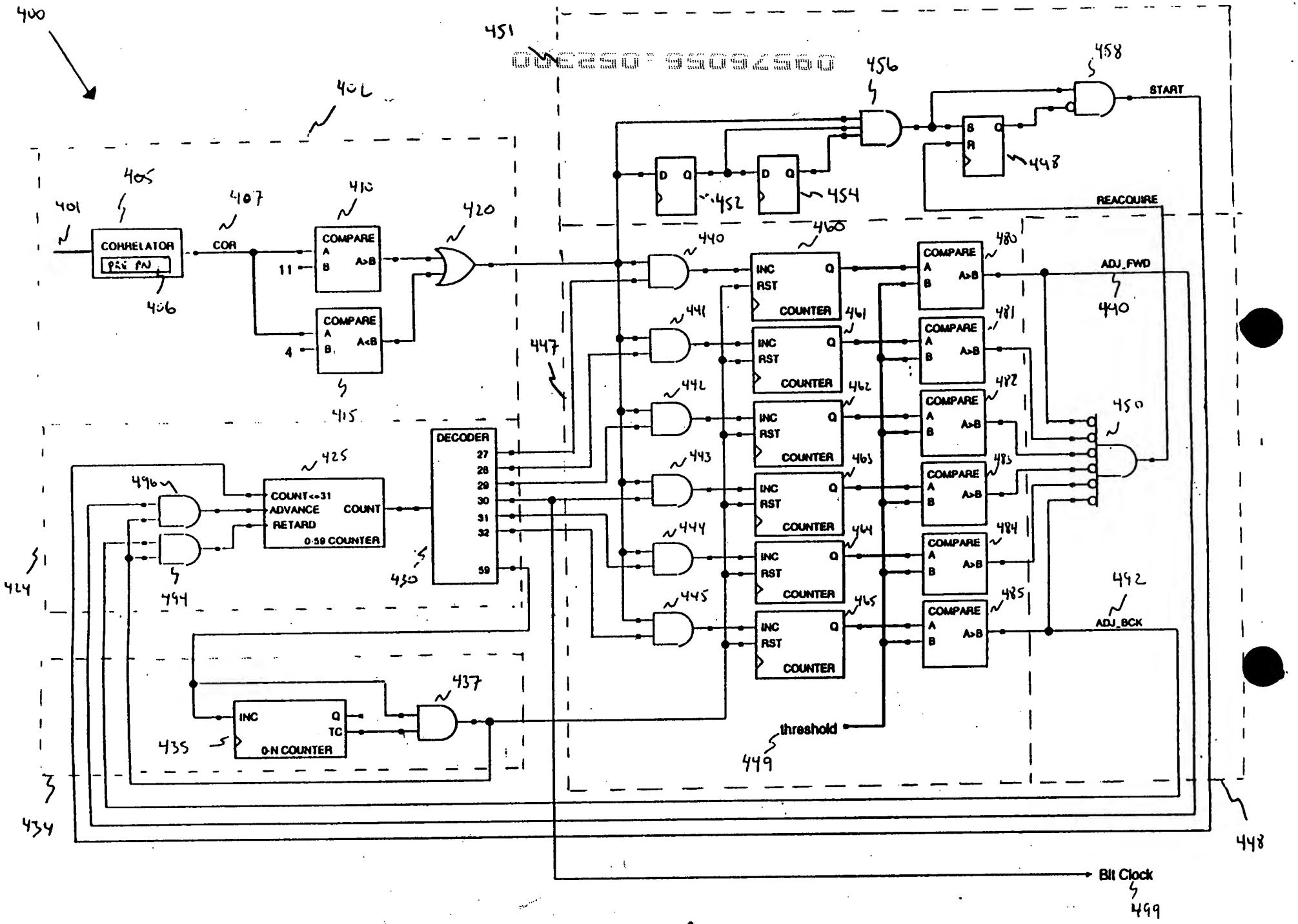

400
451
401
405
406
407
410
415
420
425
430
434
435
437
440
441
442
443
444
445
447
448
449
450
452
454
456
458
460
461
462
463
464
465
480
481
482
483
484
485
490
492
494
496
499
CORRELATOR
PSK PN
COR
COMPARE
A
B
A>B
A<B
11
4
DECODER
27
28
29
30
31
32
59
COUNT<=31
ADVANCE
RETARD
COUNT
0-59 COUNTER
INC
RST
Q
TC
COUNTER
0-N COUNTER
D
R
S
START
REACQUIRE
ADJ_FWD
ADJ_BCK
threshold
Bit Clock

Fig. 4

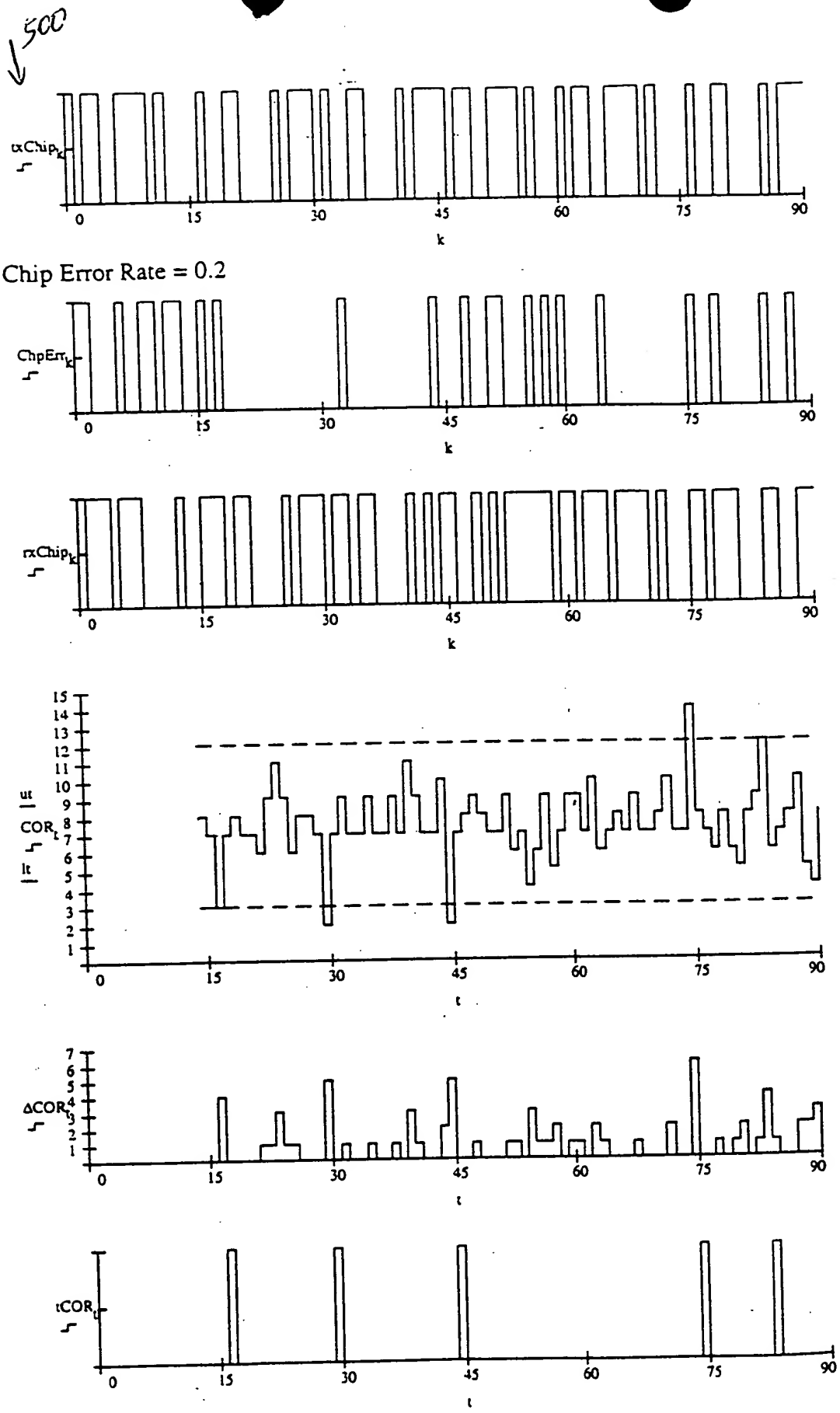

500
(a)
txChip_k
0
15
30
45
60
75
90
k
Chip Error Rate = 0.2
(b)
ChpErr_k
0
15
30
45
60
75
90
k
(c)
rxChip_k
0
15
30
45
60
75
90
k
(d)
COR_t
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
15
30
45
60
75
90
t
(e)
ΔCOR_t
7
6
5
4
3
2
1
0
15
30
45
60
75
90
t
(f)
tCOR_t
0
15
30
45
60
75
90
t

Fig. 5

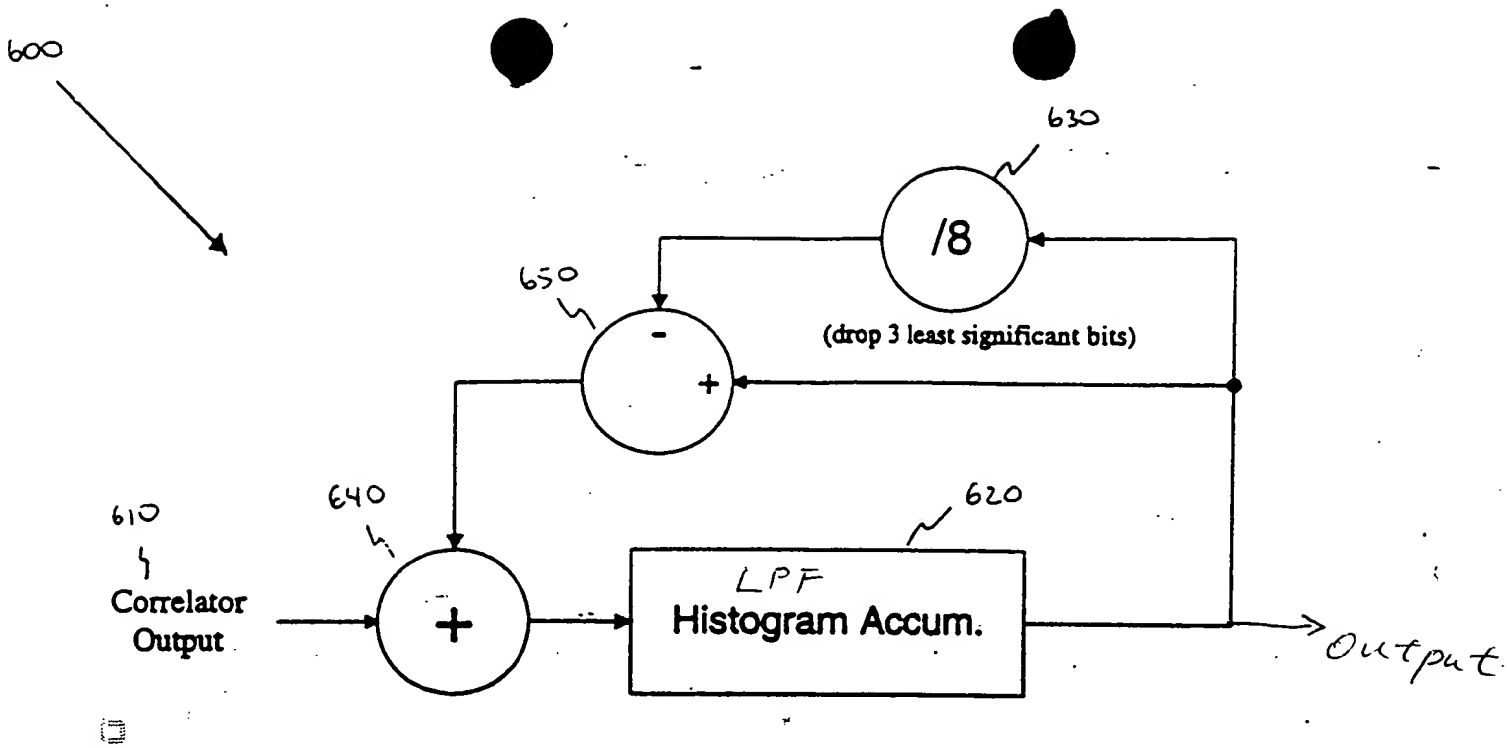
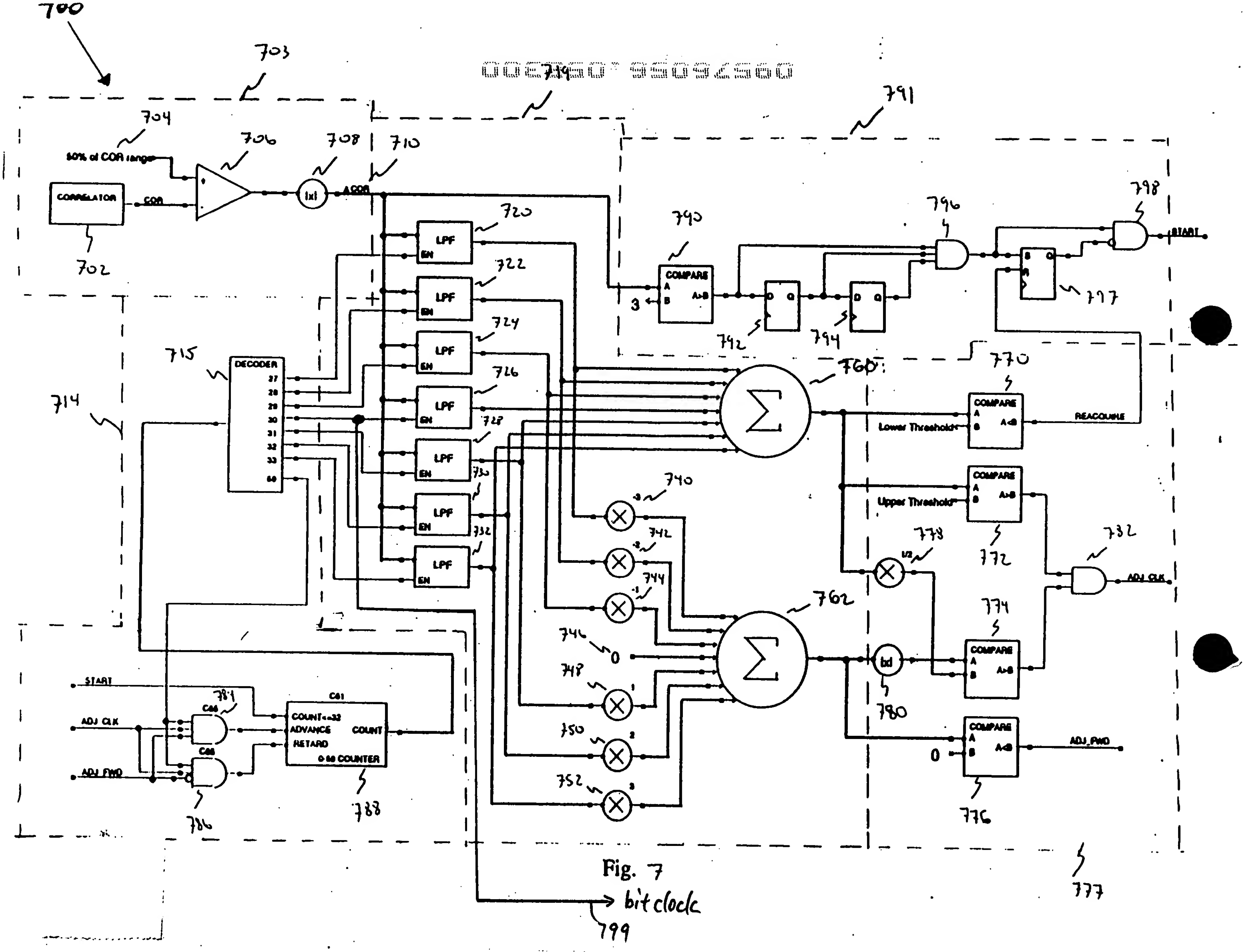

600
630
/8
650
(drop 3 least significant bits)
610
Correlator Output
640
620
LPF
Histogram Accum.
Output

Fig. 6



700
703
704
50% of COR range
706
708
710
ACOR
CORRELATOR
COR
702
714
715
DECODER
27
28
29
30
31
32
33
60
LPF
EN
720
722
724
726
728
730
732
790
COMPARE
A
B
A>B
3
792
794
796
798
START
797
S
R
Q
D
760
762
770
Lower Threshold
REACQUIRE
772
Upper Threshold
732
ADJ CLK
778
1/2
774
780
|x|
776
A<B
0
ADJ_FWD
740
742
744
746
748
750
752
-3
-2
-1
1
2
3
START
ADJ CLK
ADJ FWD
784
786
C61
COUNT<=32
ADVANCE
RETARD
COUNT
0-60 COUNTER
788
bit clock
799
777

Fig. 7

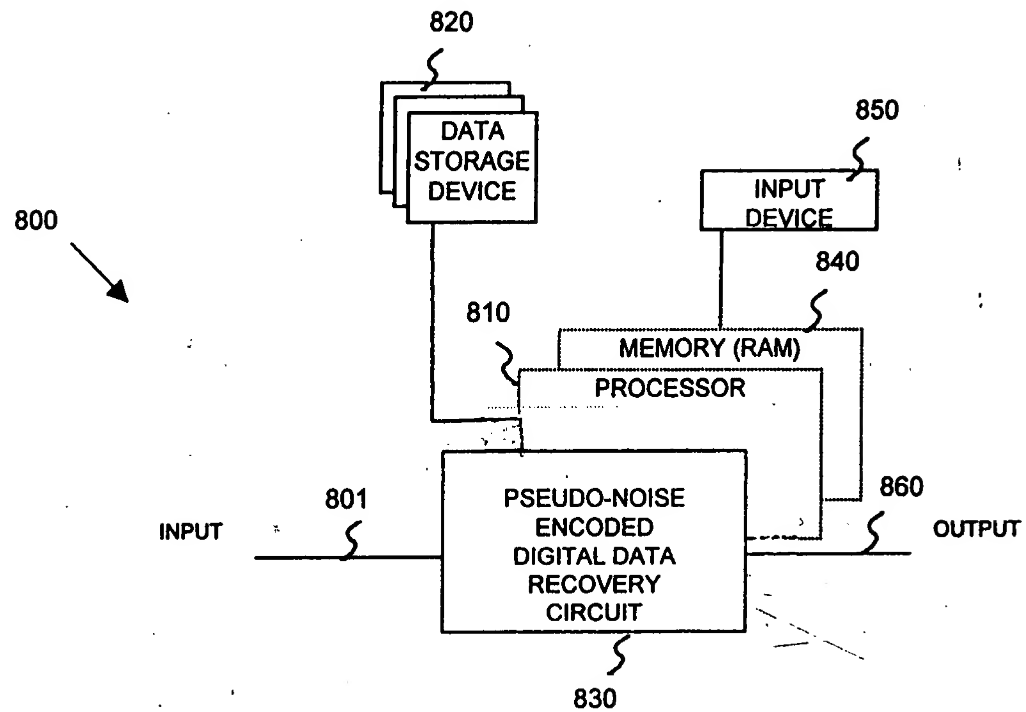


Fig. 8

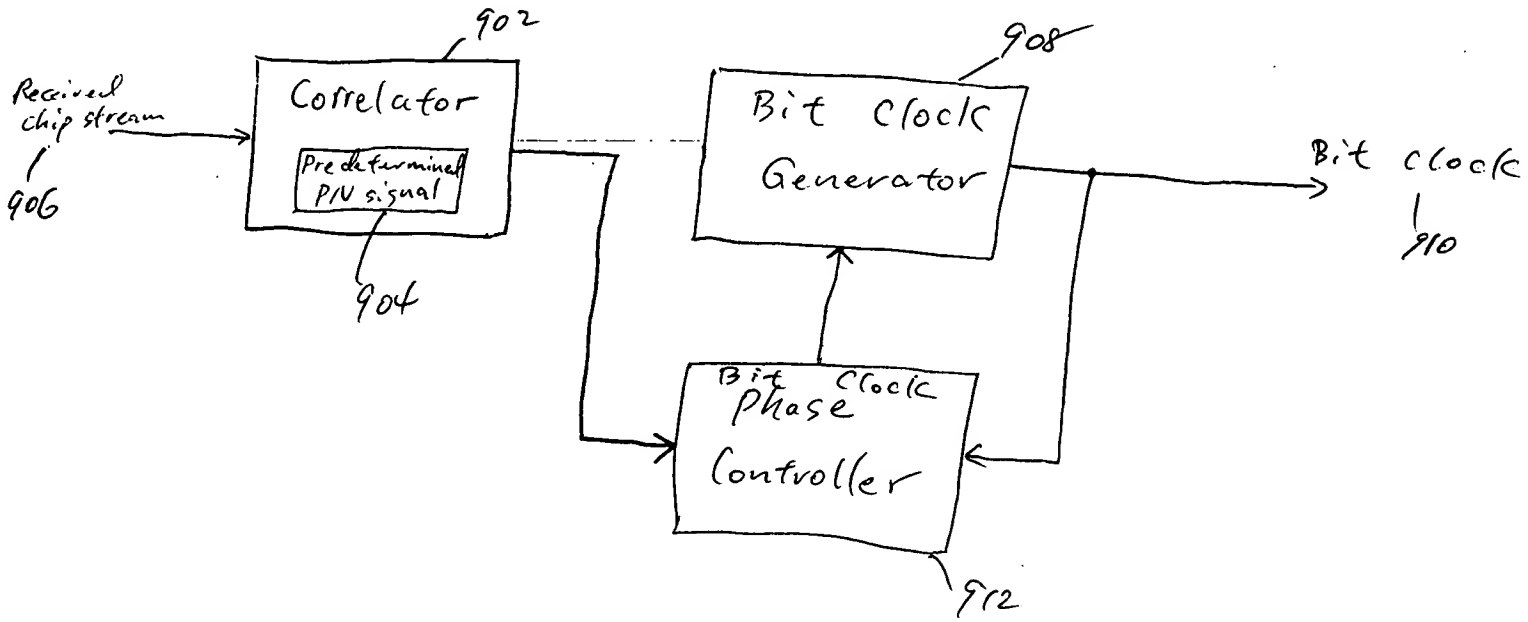

900
902
Correlator
Predetermined PN signal
904
Received chip stream
906
908
Bit Clock Generator
Bit Clock
910
Bit Clock Phase Controller
912

FIG. 9